
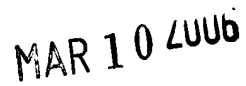
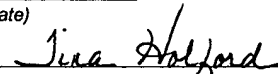


09/682 233

CFC

<b>TRANSMITTAL LETTER</b> <b>(General - Patent Issued)</b>		Docket No. <b>BUR920010042US1</b>
Patentee(s): <b>Bernstein, et al.</b>		
U.S. Patent No. <b>7,000,162</b>	Issue Date <b>February 14, 2006</b>	
Title: <b>INTEGRATED CIRCUIT PHASE PARTITIONED POWER DISTRIBUTION FOR STRESS POWER REDUCTION</b>		
<u>COMMISSIONER FOR PATENTS:</u>		
Transmitted herewith is:  <b>Certificate of Correction (2 pages)</b> <b>(USPTO Error)</b> <b>Postcard</b>		<b>Certificate</b> <b>MAR 10 2006</b> <b>of Correction</b>
<input checked="" type="checkbox"/> No additional fee is required. <input type="checkbox"/> A check in the amount of _____ is attached. <input checked="" type="checkbox"/> The Director is hereby authorized to charge and credit Deposit Account <b>09-0456 (IBM)</b> as described below. <div style="margin-left: 40px;"> <input type="checkbox"/> Charge the amount of _____  <input checked="" type="checkbox"/> Credit any overpayment.  <input checked="" type="checkbox"/> Charge any additional fee required. </div> <input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.		
<b>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</b>		
<div style="text-align: center;">   _____  <i>Signature</i> </div>		Dated: <b>03/03/2006</b>  <div style="text-align: center;">  </div>
<b>Jack P. Friedman</b> <b>Reg. No. 44,688</b> <b>Schmeiser, Olsen &amp; Watts</b> <b>3 Lear Jet Lane, Suite 201</b> <b>Latham, New York 12110</b> <b>(518) 220-1850</b>		<div style="border: 1px solid black; padding: 5px;"> I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on  <b>March 3, 2006</b>  _____  <i>(Date)</i>  <div style="text-align: center;">   _____  <i>Signature of Person Mailing Correspondence</i>  <b>Tina Holford</b>  _____  <i>Typed or Printed Name of Person Mailing Correspondence</i> </div> </div>
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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,000,162

Page 1 of 2

APPLICATION NO. : 09,682,233

ISSUE DATE : 02/14/2006

INVENTOR(S) : Bernstein, *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please add the entire "Summary of the Invention" as indicated on page 2 of 2. It was omitted in the Letters Patent.

Column 7

Line 30, delete "whore" and insert -- where --

Column 8

Line 44, delete "arc" and insert -- are --

Column 9

Line 54, delete "tail" and insert -- rail --

Column 10

Line 36, delete "front" and insert -- from --

Column 11

Line 56, delete "or" and insert -- of --

MAILING ADDRESS OF SENDER (Please do not use customer number)

Jack P. Friedman, Ph.D. Reg. No.: 44,688  
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MAR 10 2006

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,000,162

Page 2 of 2

APPLICATION NO. : 09/682,233

ISSUE DATE : 02/14/2006

INVENTOR(S) : Bernstein *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

### SUMMARY OF THE INVENTION

A first aspect of the present invention is an integrated circuit device, comprising: a first power rail for supplying power to a first latch and a circuit during a first clock phase; a second power rail for supplying power to a second latch during a second clock phase; and the circuit coupled between an output of the first latch and an input of the second latch.

A second aspect of the present invention is an integrated circuit device, comprising: a first power rail for supplying power to an L1 latch of an L1/L2 latch during a first clock phase; and a second power rail for supplying power to an L2 latch of the L1/L2 latch and to a circuit coupled to an output of the L2 latch during a second clock phase.

A third aspect of the present invention is an integrated circuit device, comprising: a first power rail for supply power to first latch and a first circuit during a first clock phase; a second power rail for supplying power to a second latch and a second circuit during a second clock phase; a third power rail for supplying power to a third latch and a third circuit during a third clock phase; a fourth power rail for supply power to fourth latch and a fourth circuit during a fourth clock phase; and the first circuit coupled between an output of the first latch and an input of the second latch, the second circuit coupled between an output of the second latch and an input of the third latch, the third circuit coupled between an output of the third latch and an input of the fourth latch and the fourth circuit coupled to an output of the fourth latch.

A fourth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supplying power to first latch and a circuit, a second power rail for supplying power to a second latch, and the circuit coupled between an output of the first latch and an input of the second latch, comprising: powering the power rail during each phase of a first clock; and powering the second power rail each phase of a second clock.

A fifth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supplying power to an L1 latch of an L1/L2 latch; and a second power rail for supplying power to an L2 latch of the L1/L2 latch and to a circuit coupled to an output of the L2 latch, comprising: powering the first power rail during each phase of a first clock; and powering the second power rail during each phase of a second clock.

A sixth aspect of the present invention is a method of stressing an integrated circuit device, the integrated circuit device including a first power rail for supply power to first latch and a first circuit, a second power rail for supplying power to a second latch and a second circuit, a third power rail for supplying power to a third latch and a third circuit, a fourth power rail for supply power to fourth latch and a fourth circuit, and the first circuit coupled between an output of the first latch and an input of the second latch, the second circuit coupled between an output of the second latch and an input of the third latch, the third circuit coupled between an output of the third latch and an input of the fourth latch and the fourth circuit coupled to an output of the fourth latch, comprising: powering the first power rail during each phase of a first clock; powering the second power rail during each phase of a second clock; powering the third power rail during each phase of a third clock; and powering the fourth power rail during each phase of a fourth clock.

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